

PHASED ARRAY CONTROLLER

The
Power
Bench

TPB 105

The Phased Array Controller (PAC) Integrated Circuit enhances the performance of power-sharing arrays of modular DC-DC converters. This device is intended for processing load share signals on the parallel bus of 2nd Generation Vicor converters. The PAC interleaves power conversion pulses produced by each module in the array, substantially reducing the peak magnitude of input reflected ripple current.

The Vicor converter topology affords a number of advantages, not the least of which is that these frequency modulated, quasi-resonant, zero current switching DC-DC converter modules lend themselves to a novel load share scheme. This method is uniquely compatible with the zero current switching topology, where line and load regulation are accomplished by controlling the rate at which pulses of energy are transferred from the primary to the secondary of the isolation transformer. The pulse width, and therefore the energy per pulse, is constant at any given input voltage. The pulse repetition rate is controlled to maintain output voltage regulation while satisfying the load current demand.

It follows therefore that identical converters in a parallel array will inherently share the load if the switching frequencies are synchronized. The switching frequency versus line/load characteristic is uniform to within 5% among modules of the same type. The PR (parallel) pin on 2nd Generation Vicor converter modules is a bidirectional port that serves as a parallel load share bus. This port can transmit or receive the synchronizing pulse signal whose leading edge is coincident with the internal power conversion pulse. One module always assumes command of the entire array, but if this module experiences a fault condition, another will take over. The PC pin, which is normally high (6V), switches low if the module shuts down. Transfer of the leadership role is completely transparent, so the output power bus is virtually unaffected by the transfer process. This feature is particularly useful in parallel arrays that employ redundancy for fault tolerance. By contrast, the pulsed synchronous current share scheme offers considerable advantages over commonly used analog methods that require either an artificial increase of the output source impedance of each converter, or a current sense device at the output of each converter.

When used with the Phased Array Controller (PAC), PR pulse processing produces a sequential distribution of the power conversion pulses generated by each module in the array. This eliminates the coherent summation of conducted and radiated EMI that is associated with the usual coincident occurrence of energy conversion pulses. The PAC is able to support up to twelve DC-DC converter modules and has dedicated input/output ports for communication with both PR and PC pins of each module, as illustrated in Figure 1. A multiplying phase-locked loop captures and locks on the PR signal from the one converter in the array that operates at the highest frequency to satisfy control equilibrium. Decoding logic sequentially provides sync pulses to PR pins of all other modules in the array whose PC pins are high.

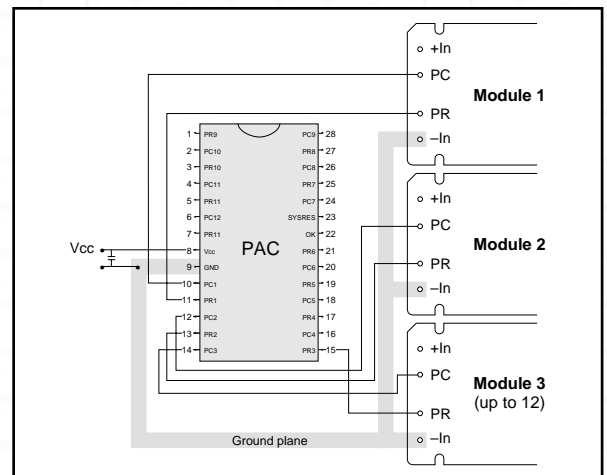


Figure 1. Interconnection of the PAC chip with three 2nd Generation DC-DC converters.

The PAC exploits the ability of Vicor converters to share the load when the operating frequencies are synchronous. The PAC, however, provides an additional benefit: phase shifted, frequency synchronous operation. That is, the sync pulses are sequentially generated with respect to the controlling converter, and delivered individually to each converter in the array, so that each generates a power conversion pulse equidistantly displaced in time, rather than simultaneously. Figure 2 illustrates a

typical PR pulse sequence for a three-module array. The apparent switching frequency of the array is therefore increased by a factor of N, where N is the number of converters in the array. More significantly, the array produces energy conversion pulses of magnitude E, as opposed to NE, which is the case when all switching occurs simultaneously.

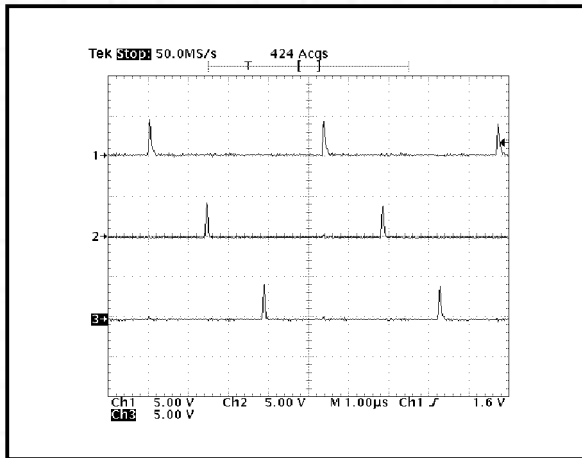


Figure 2. The PAC chip supports current sharing and adjusts the relative phase of each module in the array in increments of $360^\circ/N$, where N is the number of enabled modules within the array.

A linear relationship exists between the apparent magnitude of a power conversion pulse produced by the array, the peak reflected input ripple current and the output ripple voltage. Performance tests of converter arrays employing a PAC have demonstrated a substantial reduction in not only the magnitude of the fundamental switching frequency component, f, but also in all harmonic components generated by individual converters in the array. Equiangular phasor rotation from module to module produces a cancellation effect at the fundamental switching frequency and its harmonics, as illustrated

in Figure 3. The conducted emissions spectrum produced by an array where the PAC is employed includes components at Nf and its harmonics; each carrying upper and lower sidebands at f and its harmonics. The resulting redistribution of energy over

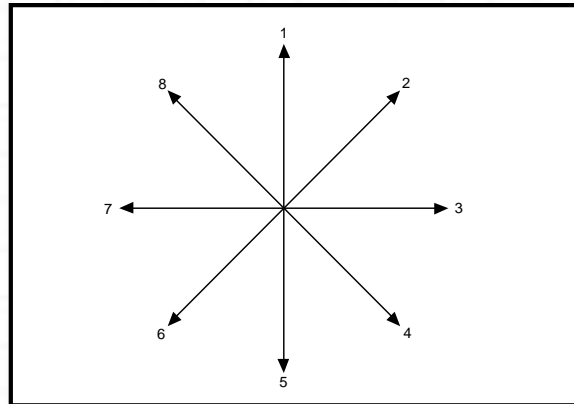


Figure 3. Vector representation of inter module phase rotation; 8-module array with PAC

a broadened and upward shifted spectrum substantially reduces the size of the input filter required to meet conducted EMI standards. Figure 4 illustrates comparative conducted emissions spectra of an eight-module array, with and without the PAC.

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Some power system applications might introduce conditions or results that differ from those described. For more information or to discuss your specific application requirements, please contact Vicor Applications Engineering at 1-800-927-9774.

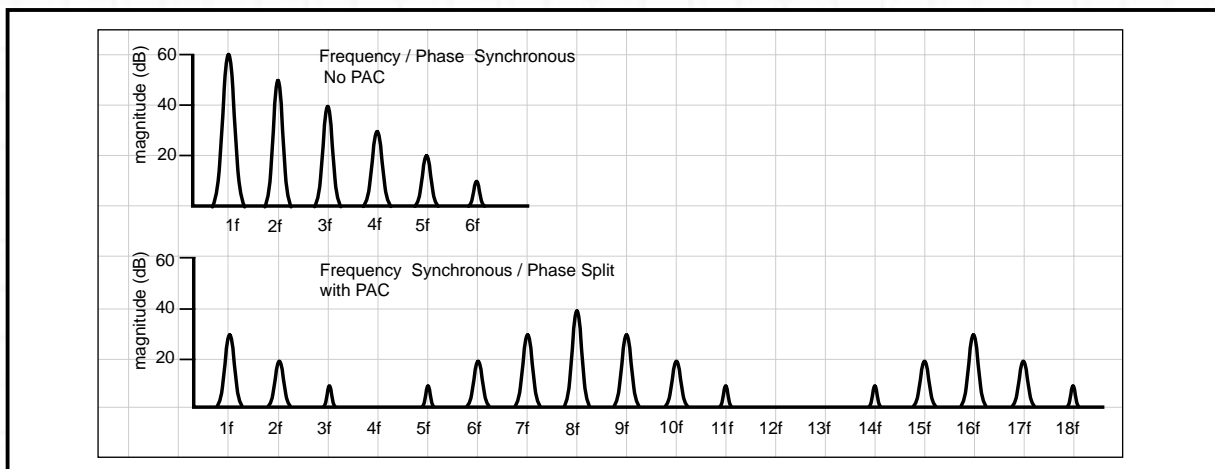


Figure 4. Conducted emissions spectrum of an 8-converter array without PAC, with PAC

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